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Design and Simulation of Wallace Tree Multiplier using Compressor

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Abstract: Low power circuit designs have been an important issue in VLSI designs areas. Multipliers play a vital role in high performance systems. The Wallace Tree Multiplier is considered as faster than simple array multiplier.WTM provides a power efficient strategy for high speed multiplication. The 4-bit Wallace tree multiplier constructed by compressor based on carry bypass or carry skip adder operation. The compressor in Wallace tree multiplier reduction can further improve the speed of multiplier. The designs are implemented in TANNER EDA Tool v13.0

Keywords: WTM, Carry Skip Adder, Compressor.

I. INTRODUCTION

Basic requirements for VLSI design are low power consumption. Compareness of the design and speed, low power will improve reliability, reduced area will improve portability and if the delay is reduced, speed will be improved. Arithmetic units are the essential blocks of digital systems such as Digital Signal Processor (DSP), Microprocessor, Microcontroller and other data processing units. For example, a study on the operation performed by Arithmetic and Logic Unit (ALU) of an ARM processor revealed that additions constituted to more than 60% of the entire mathematical operation performed which again emphasizes the importance of the multiplier block in the processors.

The objective of good multiplier is to provide a physically compact high speed and low power consumption unit. To reduce power consumption of multiplier design, it is a good direction to reduce number of operations, thereby reducing a dynamic power which s a major part of total power dissipated.

To perform binary multiplication many techniques are available and the choice depends upon some factors such as latency throughput, area and design complexity. Efficiency parallel approach uses tree of full adders to sum partial products. Wallace tree multiplier which has efficient parallel approacher and also suitable for VLSI implementations at CMOS level.

II. EXISTING SYSTEM

A.4X4 WALLACE TREE MULTIPLIER

The partial products are formed by N^2 AND gates. For the conventional Wallace reduction method, once the partial product array is formed, adjacent rows are collected into non-overlapping groups of three. Each group of three rows are reduced by

- Applying a full adder to each column that contains three bits.
- Applying a half adder to each column that contains two bits.
- Passing any single bit columns to the next stage without processing.

This reduction method is applied to each successive stage until only two rows remain. This process is illustrated by the conventional 4-bit by 4-bit Wallace tree multiplier as shown in fig 1The reduction is performed in four stages. The third phase will require a (2N-1-S) wide adder, where s- number of stages in reduction. The reduction of the Wallace tree multiplier is done by grouping the partial product as full adder and half adder.

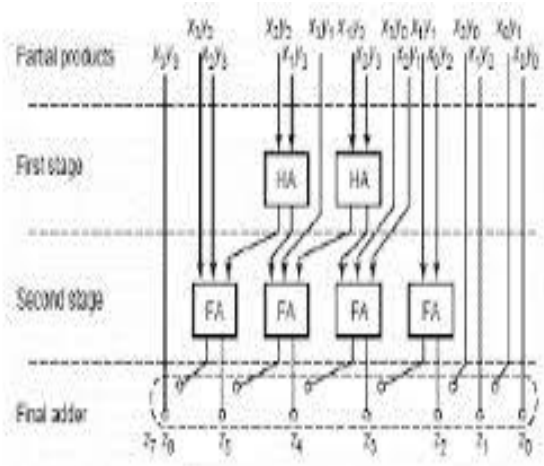

Figure (1) Wallace Tree Circuit

B. COMPRESSOR ARCHITECTURE BASED CARRY LOOK AHEAD ADDER

The existing architecture aims to reduced the power consumption by make design use of compressor in place of full adders. The 6:3 compressor is used logic of carry look ahead adder which uses propagate and generate

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signals to speed up the addition. The Wallace tree multiplier reduction stage in partial products, the full adder can be replaced with compressor of 6:3 based carry look ahead operation. Instead of propagating carry through all stages of adder, it calculates all carrier in parallel manner and flow diagram for the CLA adder is given in fig 3.4,

- G_i be the generate for the i^{th}bit
- P_i be the propagate for the i^{th} bit.

If the carry generate G_i is true,then carry is generated at the i^{th}bit. If the carry propagate,$P_i$is true,then carry-into the i_{th} bit is propagated to the carry-in of i_{th+1} bit.
The equations is given by,
$G_i = A_i.B_i$
$P_i = A_i$xor B_i
$C_i = G_i + P_i.C_i$

- $S_i = P_i$ xorC_i

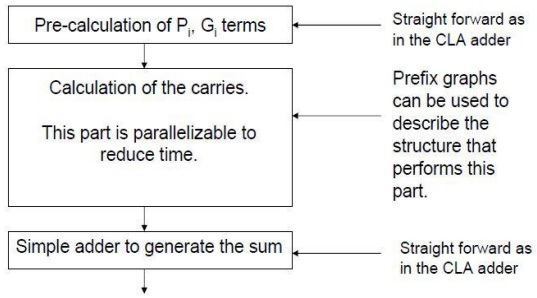

Figure (2) Different Stages Of CLA Operation .

WALLACE TREE MULTIPLIER BASED CLA COMPRESSOR

The Wallace tree multiplier based CLA compressor is simulated using Tanner EDA tool as shown in figure 3.

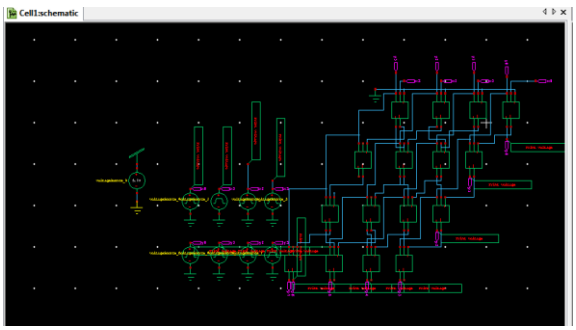

Figure (3) WTM Based CLA Compressor

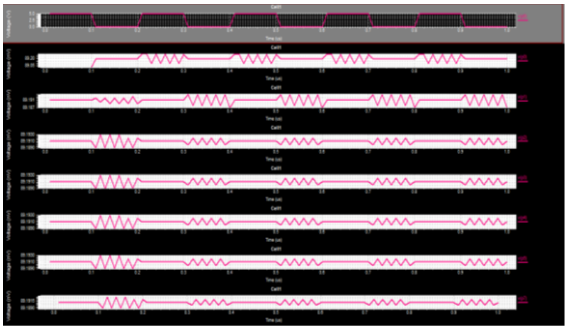

Figure (4) Output Waveform

III. PROPOSED SYSTEM

In this proposed system, the Wallace tree multiplier using 6:3 compressor based carry skip adder (or) carry bypass adder. In this proposed system, we have taken care of problems. For achieving performance enhancement of multiplier.

CARRY BYPASS ADDER (OR) CARRY SKIP ADDER

Carry skip adder contains carry skip circuitry which contains two logic gate, one AND gate and one OR gate. AND gate accepts the carry-in-bit and compares it to the group propagate signal, output of the AND gate is ORed with C_{i+1} to produce stage output. The propagate and carry output are

$$P_{[i,i+3]}=P_{i+3}.P_{i+2}.P_{i+1}.P_i$$
$$Carry = C_{i+4} + P_{[i,i+3]}.C_i$$

The carry skip adder (or) carry bypass adder block as shown in figure 5& 6.

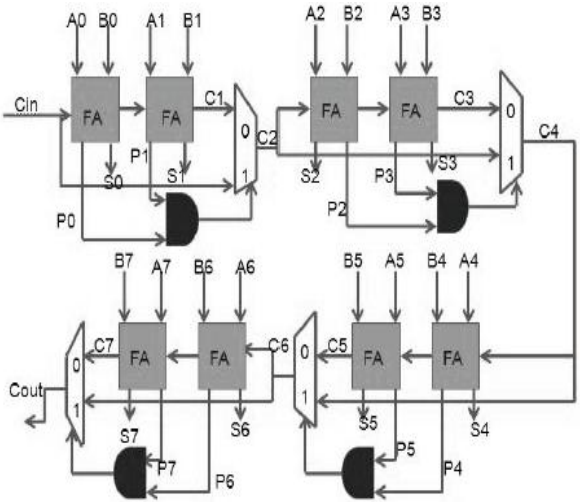

Figure (5) Blocks of Carry Skip Adder

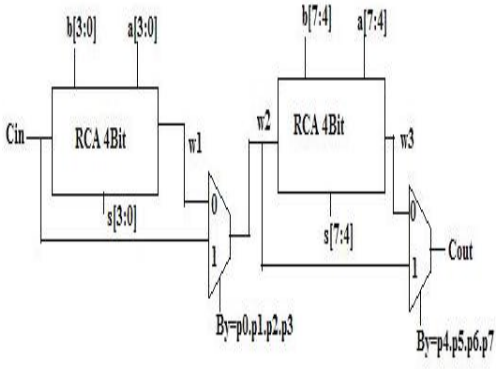

Figure (6) Blocks of Carry Bypass Adder

Two conditions based on the propagation term,
[1] $P_{[i,i+3]}=0$ - carry output is determined by $C_{i+4.}$
[2] $P_{[i,i+3]}=1$ - when C_{in} bit $C_i=1$, then group carry is automatically sent to the next group of adders. Here carry-in-bit skips carry in the block entirely.

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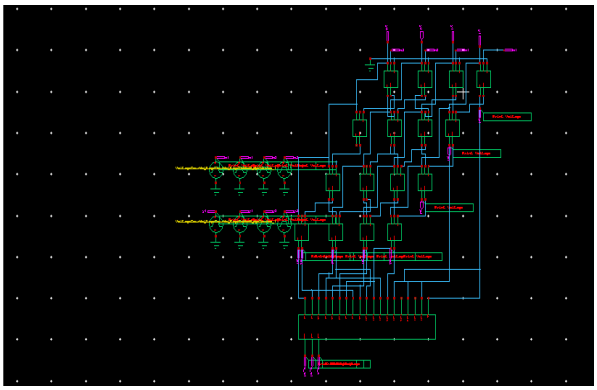
WALLACE TREE USING CBA COMPRESSOR DESIGN

The proposed architecture for a Wallace tree multiplier using CBA compressor as shown in figure 7.



Figure(7) WTM based CBA compressor

SIMULATION OUTPUT

The simulation output waveform for the Wallace tree multiplier using CBA based compressor as shown in figure 8& 9.

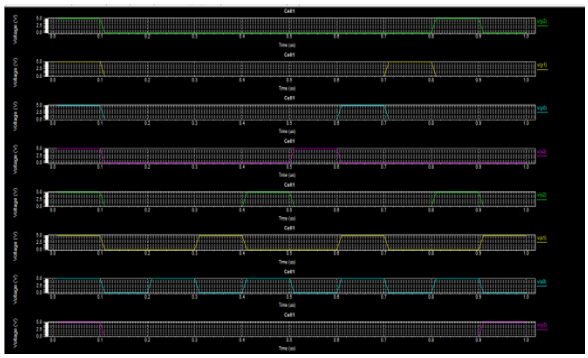


Figure (8) Output Waveform

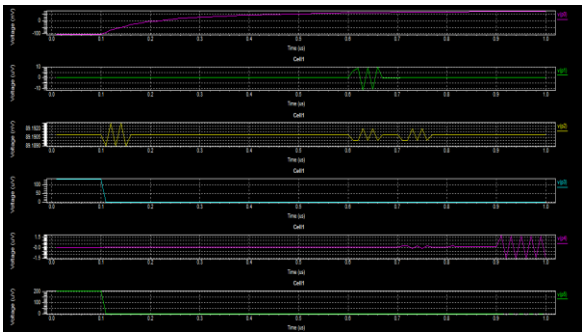


Figure (9) Output Waveform

TABLE I COMPARISON OF POWER RESULTS

CONVENTIONAL WALLACE TREE MULTIPLIER	6.08188*10-3 watts
WALLACE TREE MULTIPLIER USING CLA COMPRESSOR	3.949628*10-6 watts
WALLACE TREE MULTIPLIER USING CBA COMPRESSOR	1.53270*10-2 watts

CONCLUSION

It is concluded from above that power consumption is minimum in case of Wallace tree multiplier based Carry bypass adder based compressor. In case of Carry look ahead adder, carry expression becomes complex compared to Wallace tree multiplier based carry bypass adder. In this adder bypass logic has been used to reduce switching activity. As a result delay and power consumption has been reduced.

REFERENCES

[1] Christopher S.Wallace. "A Suggestion for a Fast Multiplier", IEEE Transactions on Electronic Computers, Volume: EC-13, No. 1, pp. 14-17, February 1964.

[2] S.Karthick, S.Karthika, S.Valarmathy. "Design and Analysis of Low Power Compressors", International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering, Vol. 1, Issue: 6, December 2012

[3] Ravi Nirlakalla, ThotaSubbaRao, TalariJayachandra Prasad. "Performance Evaluation of High Speed Compressors for High Speed Multipliers", Serbian Journal of Electrical Engineering, Vol. 8, No. 3, November 2011, 293-306.

[4] KhushbooBais, Zoonubiya Ali. "Design of a High-Speed Wallace Tree Multiplier", International Journal of Engineering Sciences & Research Technology, Vol. 5, No. 6, June 2016.

[5] HimanshuBansal, K.G.Sharma, Tripti Sharma. "Wallace Tree Multiplier Designs: A Performance Somparison Review", Innovative Systems Design and Engineering, Vol. 5, No. 5, 2014.

[6] J.Rabaey, A.Chandrakasan, B.Nikolic. "VLSI Digital Circuits", CMPEN 411, Spring 2012, (Adapted from Rabaey's Digital Integrated Circuits, Second Edition, ©2003).

[7] "Guide to the Tanner EDA Design Tools", Version 12.6, Montana State University, User's Manual, 2011, copyright.

[8] AnaghP.Deshpande, AmeyaA.Chandras, Dr. Vigneswaran.T. "An Efficient Implementation of Wallace Tree Multiplier", International Journal on Recent and Innovation Trends in Computing and Communication, Vol. 4, Issue: 3, March 2016.

[9] Naveen Kr.Gahlan. "Implementation of Wallace Tree Multiplier using Compressor", International Journal of Computer Technology and Applications, Vol. 3, No. 3, May-June 2012.

[10] ShahzadAsif, Yinan Kong. "Design of an Algorithmic Wallace Multiplier using High Speed Counters", In Computer Engineering & Systems (ICCES), 2015 Tenth International Conference on, pp. 133-138, IEEE, 2015.

[11] ShahzadAsif, Yinan Kong. "Analysis of different architectures of counter based Wallace multipliers", In Computer Engineering & Systems (ICCES), 2015 Tenth International Conference on, pp. 139-144, IEEE, 2015.

[12] Soniya, Suresh Kumar, "A Review on Different Type of Multipliers And Multiplier-Accumulator Unit", International Journal of Emerging Trends & Technology in Computer Science (IJETTCS), Vol. 2, No. 4, pp. 364-368, July-August, 2013.

[13] Jatinder Kumar, "Design and Comparative Analysis of CMOS Full Adder Cells Using Tanner EDA Tool", International Journal of Computer Science and Engineering Technology, Vol. 5, No. 2, pp. 71-79, 2014.

[14] K.Gopi Krishna, B.Santhosh, V.Sridhar, "Design of Wallace Tree Multiplier using Compressors", International Journal of Engineering Sciences and Research Technology, Vol. 2, No. 9, pp. 2249-2254, September 2013.

[15] SumitVaidya, Deepak Dandekar, "Delay-Power Performance Comparison of Multipliers in VLSI Circuit Design", International Journal of Computer Networks & Communications (IJCNC), Vol. 2, No. 4, July 2010.

[16] JasbirKaur, LalitSood, "Comparison Between Various Types of Adder Topologies", IJCST, Vol. 6, Issue: 1, January – March 2015.